Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-11. (Canceled)

12. (New) A differential circuit comprising:

a first transistor that has a first drain and a first source;

a capacitor that is connected to a first gate of the first transistor;

a first switch that controls an electrical connection between the first gate and the first drain;

a second transistor that has a second drain and a second source and is connected to the first transistor; and

a second switch, a third switch and a fourth switch respectively applying first, second and third independent voltages to a second gate of the second transistor,

the differential circuit being configured such that in a first period the first gate is electrically connected to the first drain through the first switch and the first independent voltage is applied to the second gate through the second switch,

in a second period the second independent voltage is applied to the second gate through the third switch, and

in a third period the third independent voltage is applied to the second gate through the fourth switch,

none of the first, second and third periods overlapping.

13. (New) The differential circuit according to claim 12, wherein the

differential circuit is configured such that a first current flows through the first transistor and the second transistor during the first period.

14. (New) The differential circuit according to claim 12, wherein the differential circuit is configured such that a second current flows through the first transistor and the second transistor during the second period.

15. (New) The differential circuit according to claim 12, wherein the differential circuit is configured such that the second transistor functions as a current source.

16. (New) The differential circuit according to claim 12, wherein the differential circuit is configured such that the first switch and the second switch are controlled by an identical signal.

17. (New) The differential circuit according to claim 12, further comprising an amplifier that is connected to the first transistor.

18. (New) The differential circuit according to claim 12, wherein the differential circuit is configured such that any one of the second drain and the second source is electrically connected to a predetermined potential.

19. (New) The differential circuit according to claim 13, wherein the differential circuit is configured such that a charge corresponding to the first current is charged to the capacitor during the first period.

20. (New) The differential circuit according to claim 12, wherein the differential circuit is configured such that the differential circuit amplifies an output of a sensor pixel.

21. (New) An electronic device comprising the differential circuit according to

claim 12.

22. (New) The differential circuit according to claim 12, a first period being provided between each of the second and third periods.

23. (New) A differential circuit comprising:

a first transistor that has a first drain and a first source;

a capacitor that is connected to a first gate of the first transistor;

a first switch that controls an electrical connection between the first gate and the first drain;

a second transistor that has a second drain and a second source;

a second switch, and a third switch that are connected in parallel and control an electrical connection between the first transistor and the second transistor; and

a fourth switch and a fifth switch respectively applying first and second independent voltages to a second gate of the second transistor,

the differential circuit being configured such that in a first period the first gate is electrically connected to the first drain through the first switch, the first transistor is electrically connected to the second transistor through the second switch and the first independent voltage is applied to the second gate through the fourth switch, and

in a second period the first transistor is electrically connected to the second transistor through the third switch and the second independent voltage is applied to the second gate through the fifth switch,

the first and second periods being non-overlapping.